Reversible computer hardware

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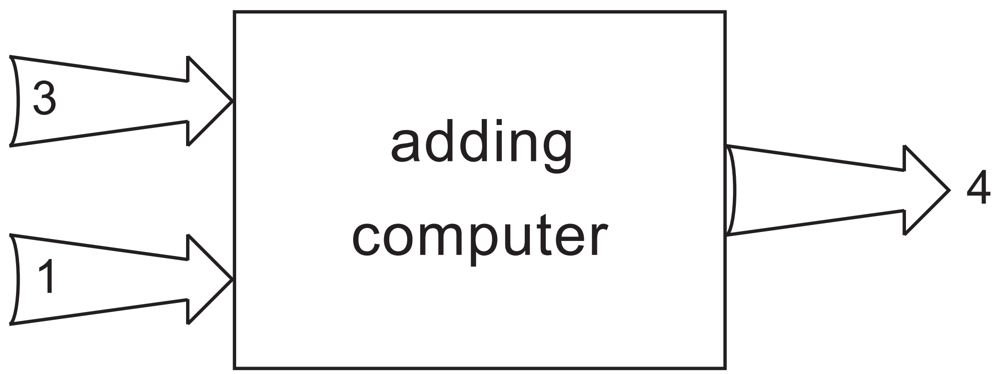
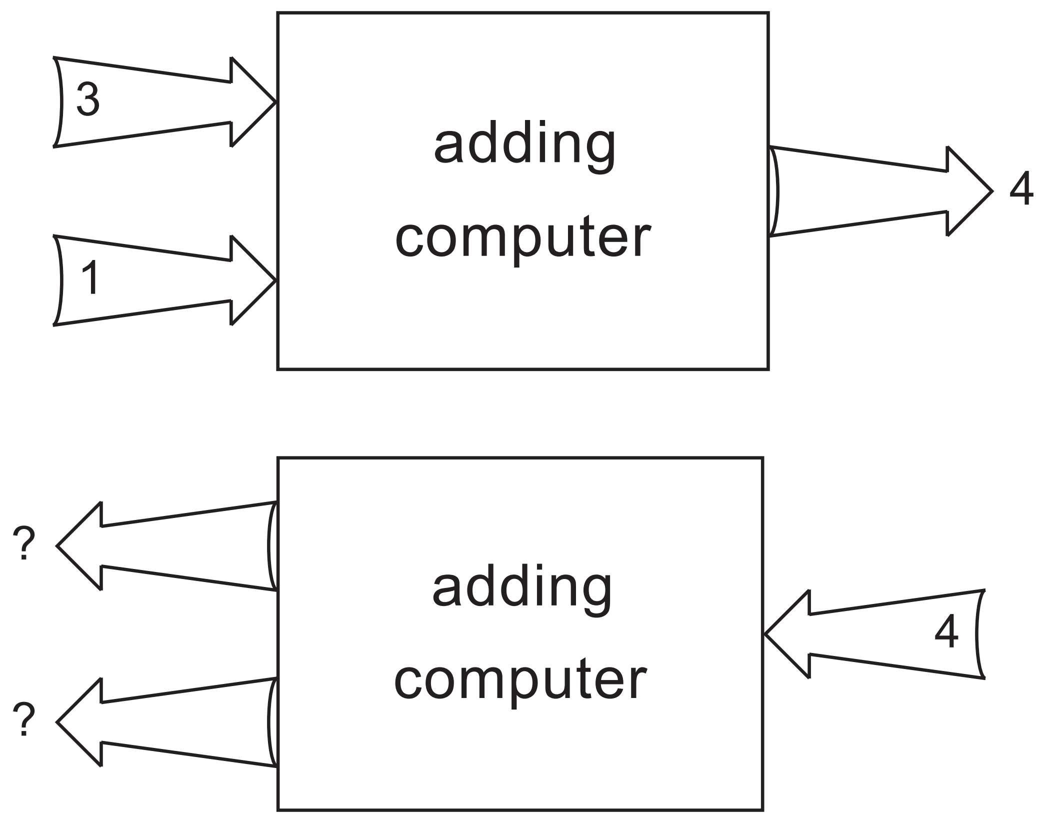
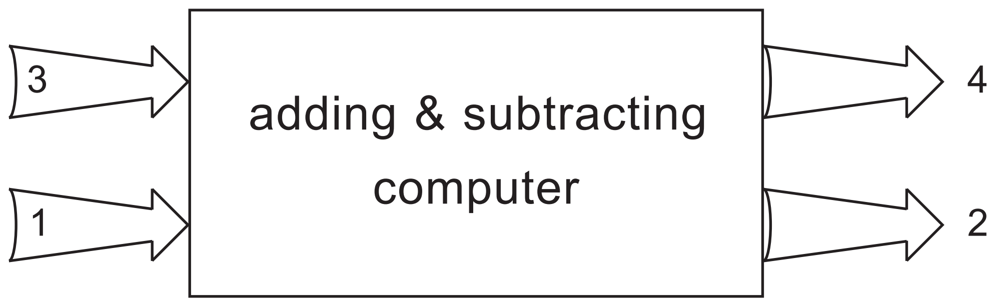
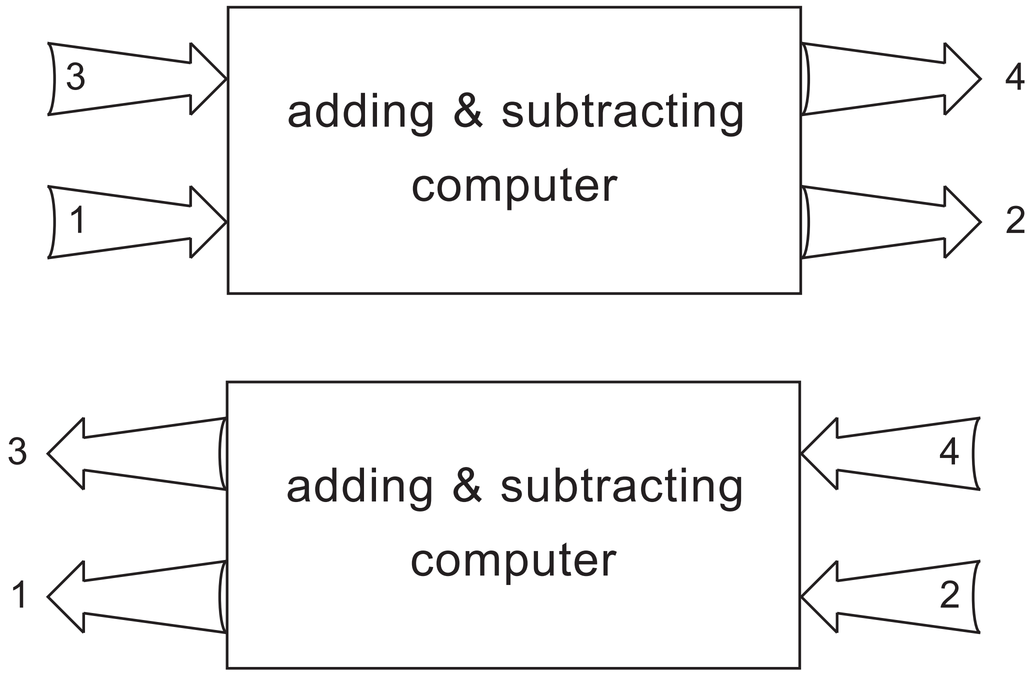
A logically irreversible computer

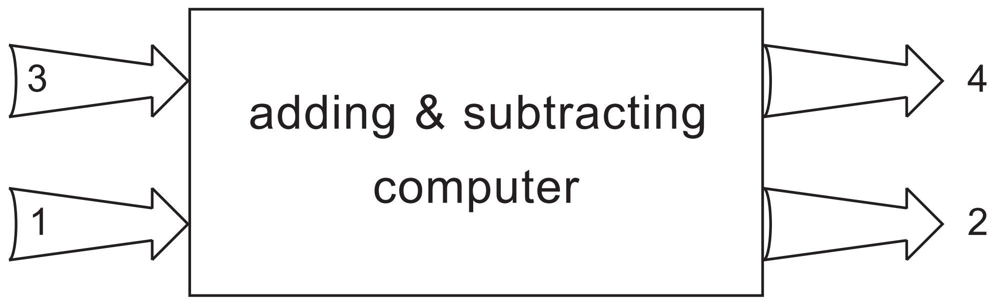


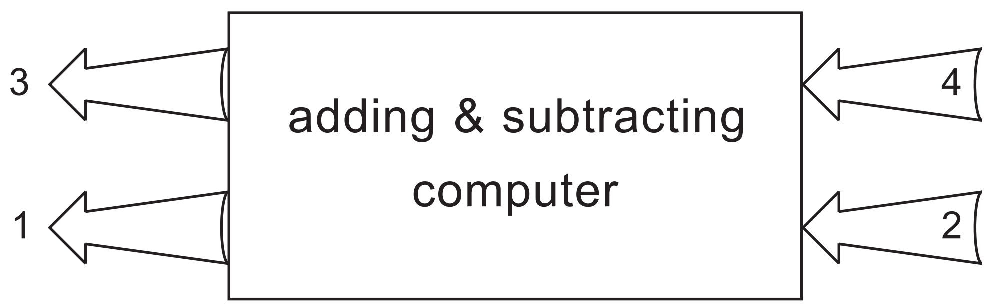

3
1
adding
computer
4
?
?
adding
computer
4

A logically reversible computer :




3
1
adding & subtracting computer
4
2
3
1
adding & subtracting computer
4
2





$$\begin{cases} P &= A + B \\ Q &= A - B \end{cases}$$

$$\Rightarrow \begin{cases} A &= \frac{1}{2}\,P + \frac{1}{2}\,Q \\ B &= \frac{1}{2}\,P - \frac{1}{2}\,Q \end{cases}$$

Truth table of three irreversible logic gates
(a) `XOR` gate
(b) `NOR` gate
(c) `AND` gate.

AB	P
0 0	0
0 1	1
1 0	1
1 1	0

(a)

$P = A \oplus B$

AB	P
0 0	1
0 1	0
1 0	0
1 1	0

(b)

$P = \overline{A + B}$

AB	P
0 0	0
0 1	0
1 0	0
1 1	1

(c)

$P = A\ B$

Truth table of a reversible logic gate

AB	PQ
0 0	0 0
0 1	1 0
1 0	1 1
1 1	0 1

$P = A \oplus B$
$Q = A$

Groups

A group G consists of :

- **a set S and**
- **an operation Ω .**

Set and operation have to fulfil conditions :

- **S has to be closed :**
  $a \ \Omega \ b \in S$
- **Ω has to be associative :**
  $(a \ \Omega \ b) \ \Omega \ c = a \ \Omega \ (b \ \Omega \ c)$
- **S has to have an identity element :**
  $a \ \Omega \ i = a$
- **each element of S has to have an inverse in S :**
  $a \ \Omega \ a^{-1} = i$

Truth table of three reversible logic gates of width 2
(a) an arbitrary reversible gate r
(b) the identity gate i
(c) the inverse r^{-1} of r

AB	PQ
0 0	0 0
0 1	1 0
1 0	1 1
1 1	0 1

(a)

AB	PQ
0 0	0 0
0 1	0 1
1 0	1 0
1 1	1 1

(b)

AB	PQ
0 0	0 0
0 1	1 1
1 0	0 1
1 1	1 0

(c)

The group of reversible gates of width w is isomorphic to the symmetric group $\mathbf{S}_{2^w}$.
Its order is $(2^w)!$.

Here $w = 2$
Thus $\mathbf{S}_4$
Its order is 4! = 24.

Truth table of reversible logic gates ($w = 3$)
(a) an arbitrary one
(b) a twin gate
(c) a control gate

ABC	PQR
0 0 0	1 0 0
0 0 1	0 0 0
0 1 0	0 0 1
0 1 1	1 0 1
1 0 0	1 1 1
1 0 1	0 1 1
1 1 0	0 1 0
1 1 1	1 1 0

(a)

ABC	PQR
0 0 0	0 1 0
0 0 1	0 0 0
0 1 0	0 1 1
0 1 1	0 0 1
1 0 0	1 1 0
1 0 1	1 1 1
1 1 0	1 0 1
1 1 1	1 0 0

(b)

ABC	PQR
0 0 0	0 0 1
0 0 1	0 0 0
0 1 0	0 1 0
0 1 1	0 1 1
1 0 0	1 0 0
1 0 1	1 0 1
1 1 0	1 1 1
1 1 1	1 1 0

(c)

$a \in \mathbf{S}_8$
$b \in \mathbf{S}_4 \times \mathbf{S}_4$
$c \in \mathbf{S}_2 \times \mathbf{S}_2 \times \mathbf{S}_2 \times \mathbf{S}_2$

The subgroup of control gates

$$\begin{aligned} P &= A \\ Q &= B \\ R &= f(A,B) \oplus C \ . \end{aligned}$$

ABC	PQR
0 0 0	0 0 0
0 0 1	0 0 1
0 1 0	0 1 1
0 1 1	0 1 0
1 0 0	1 0 0
1 0 1	1 0 1
1 1 0	1 1 1
1 1 1	1 1 0

(a)

ABC	PQR
0 0 0	0 0 0
0 0 1	0 0 1
0 1 0	0 1 0
0 1 1	0 1 1
1 0 0	1 0 0
1 0 1	1 0 1
1 1 0	1 1 1
1 1 1	1 1 0

(b)

Examples :
(a) $f(A,B) = B$
(b) $f(A,B) = AB$ **: the `TOFFOLI` gate.**

This subgroup of control gates is isomorphic to the Young subgroup $\mathbf{S}_2 \times \mathbf{S}_2 \times ... \times \mathbf{S}_2 = \mathbf{S}_2^{2^{w-1}}$.

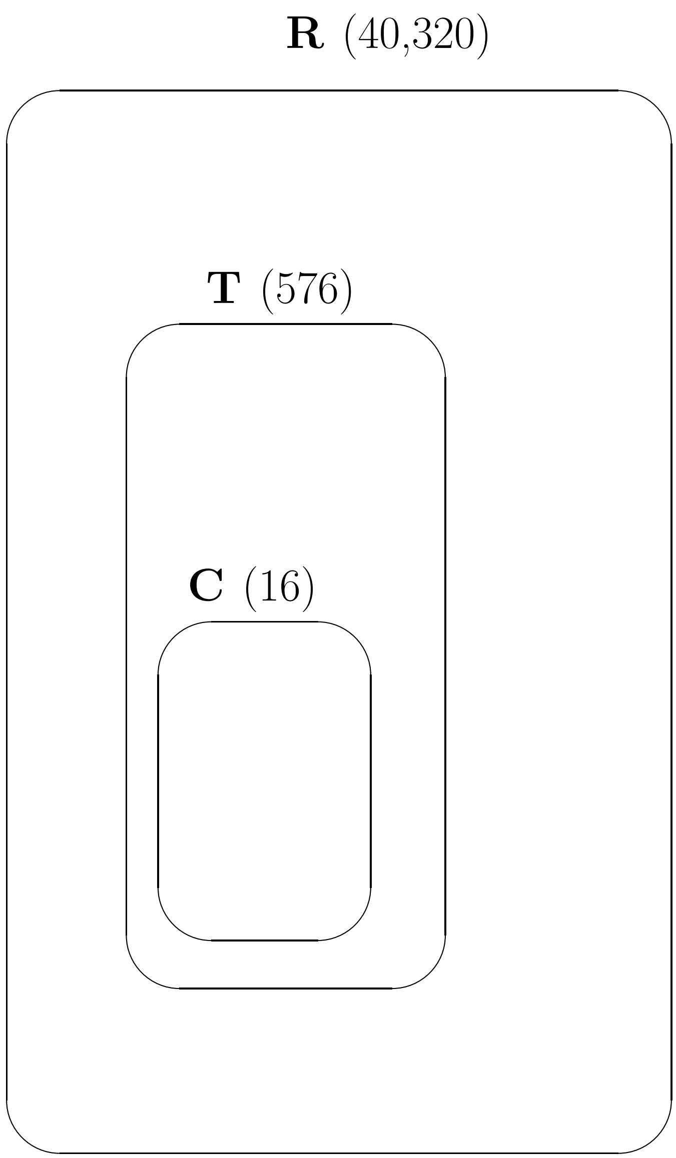
Here $w = 3$
Thus $\mathbf{S}_2 \times \mathbf{S}_2 \times \mathbf{S}_2 \times \mathbf{S}_2 = \mathbf{S}_2^4$
Its order is $2^4 = 16$.

The number r of reversible gates,
the number t of twin gates,
the number c of control gates

w	r	t	c
1	2	1	2
2	24	4	4
3	40,320	576	16
4	20,922,789,888,000	1,625,702,400	256

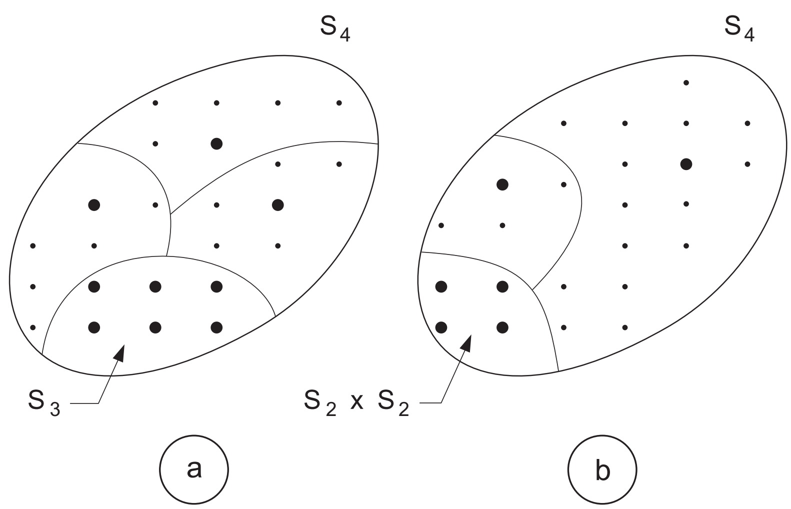
$$r(w) = (2^w)!$$
$$t(w) = [(2^{w-1})!]^2$$
$$c(w) = (2!)^{2^{w-1}} = 2^{2^{w-1}}$$

$w = 3$



Cosets

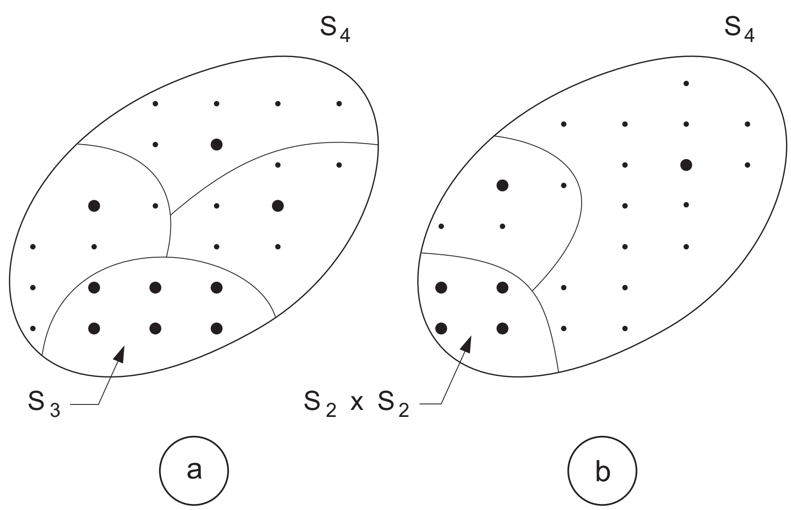
Let a be a member of the group $\mathbf{G}$.
The coset of a is the set $b\,\Omega\,a$,
where b is a member of the subgroup $\mathbf{H}$.



The symmetric group $\mathbf{S}_4$ partitioned
(a) as the four left cosets of $\mathbf{S}_3$.

Double cosets

Let a be a member of the group $\mathbf{G}$.
The double coset of a is $b_1 \; \Omega \; a \; \Omega \; b_2$,
where both b_1 and b_2 are members of subgroup $\mathbf{H}$.



The symmetric group $\mathbf{S}_4$ partitioned
(a) as the four left cosets of $\mathbf{S}_3$
(b) as the three double cosets of $\mathbf{S}_2{\times}\mathbf{S}_2$.

Double cosets

The double coset of a is $b_1 \; \Omega \; a \; \Omega \; b_2$,
where both b_1 and b_2 are members of subgroup $\mathbf{H}$.

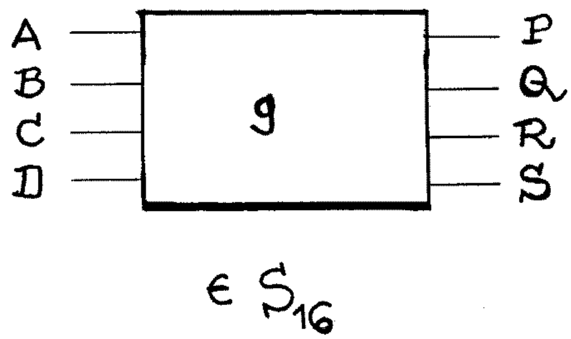
The twin gates lead to a
chain of subgroups:

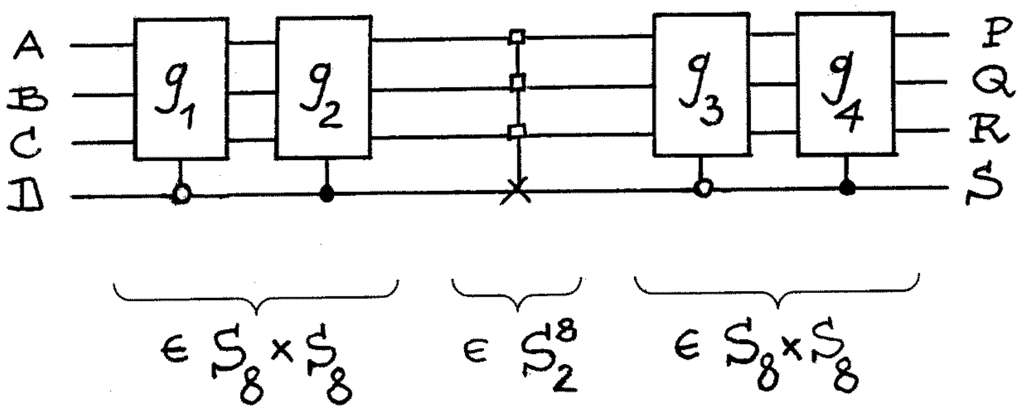
$$\mathbf{S}_8 \supset \mathbf{S}_4^2 \supset \mathbf{S}_2^4 \supset \mathbf{S}_1^8 = \mathbf{I} \quad .$$

with subsequent orders

$$40,320 > 576 > 16 > 1 \; .$$

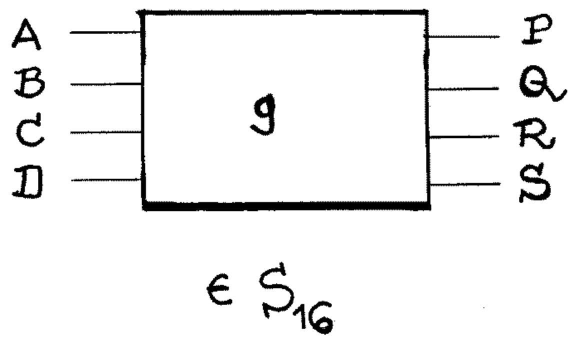
For synthesizing all 40,320 members of $\mathbf{S}_8$,
they need a library of only 7 elements.
The synthesis is a cascade with length of 7 or less.

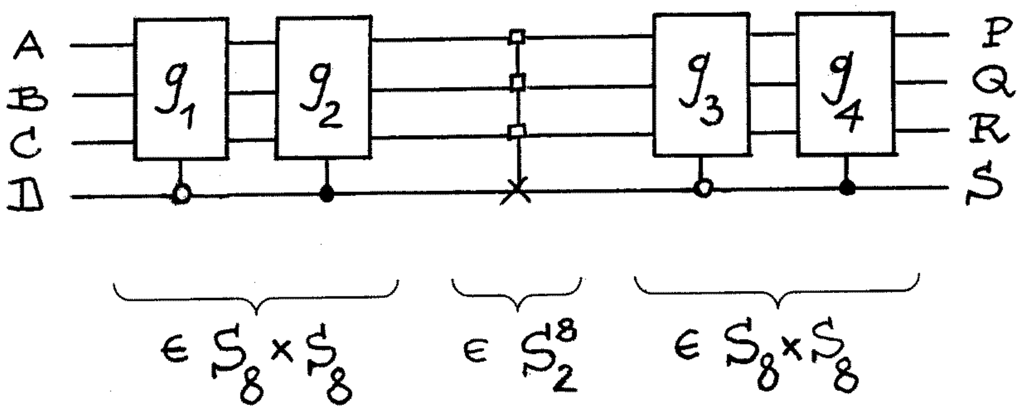




Synthesis according to
double coset space

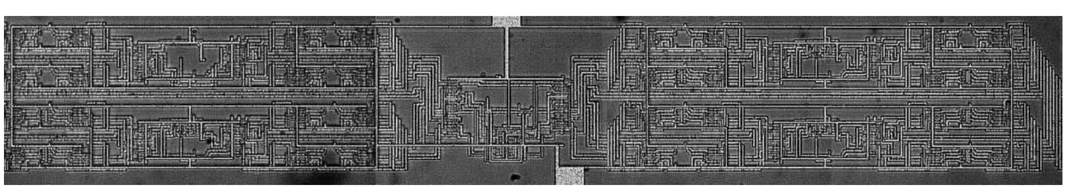
$\mathbf{S}_8\times \mathbf{S}_8 \backslash \mathbf{S}_{16} / \mathbf{S}_8\times \mathbf{S}_8$



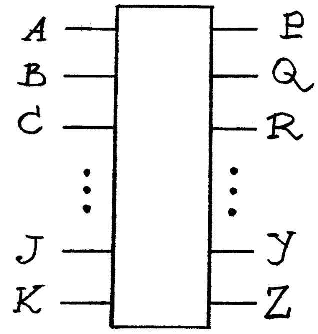


Synthesis according to
double coset space

$\mathbf{S}_8\times\,\mathbf{S}_8\backslash\,\mathbf{S}_{16}\;/\;\mathbf{S}_8\times\,\mathbf{S}_8$



Electronics



Electronic implementation is based on
the subgroup of control gates :
w inputs A, B, C, ..., J, and K and
w outputs P, Q, R, ..., Y, and Z, such that :

$$\begin{aligned} P &= A \\ Q &= B \\ R &= C \\ ... &= ... \\ Y &= J \\ Z &= f(A, B, C, ..., J) \oplus K \ , \end{aligned}$$

where f is an arbitrary boolean function
of the $w-1$ variables A, B, C, ..., J.

The subgroup is isomorphic to $\mathbf{S}_2^{2^{w-1}}$ of order $2^{2^{w-1}}$.

Three special examples:

- If $f = 0$, then $Z = K$.
  Then the gate is the identity gate i.
- If $f = 1$, then $Z = 1 \oplus K = \overline{K}$.
  Then the gate is the inverter or `NOT` gate.
- If $f(A, B, C, ..., J) = ABC...J$,
  then the gate is the `CONTROLLED`$^{w-1}$ `NOT` gate
  or `TOFFOLI` gate.

The `NOT` gate:

$$P = \overline{A}$$

The `CONTROLLED NOT` gate:

$$\begin{aligned} P &= A \\ Q &= A \oplus B \ . \end{aligned}$$

is equivalent with

$$\begin{aligned} P &= A \\ Q &= \textbf{if } (A = 0) \textbf{ then } B \textbf{ else } \overline{B} \ . \end{aligned}$$

The `CONTROLLED CONTROLLED NOT` gate or `TOFFOLI` gate:

$$\begin{aligned} P &= A \\ Q &= B \\ R &= AB \oplus C \ . \end{aligned}$$

is equivalent with

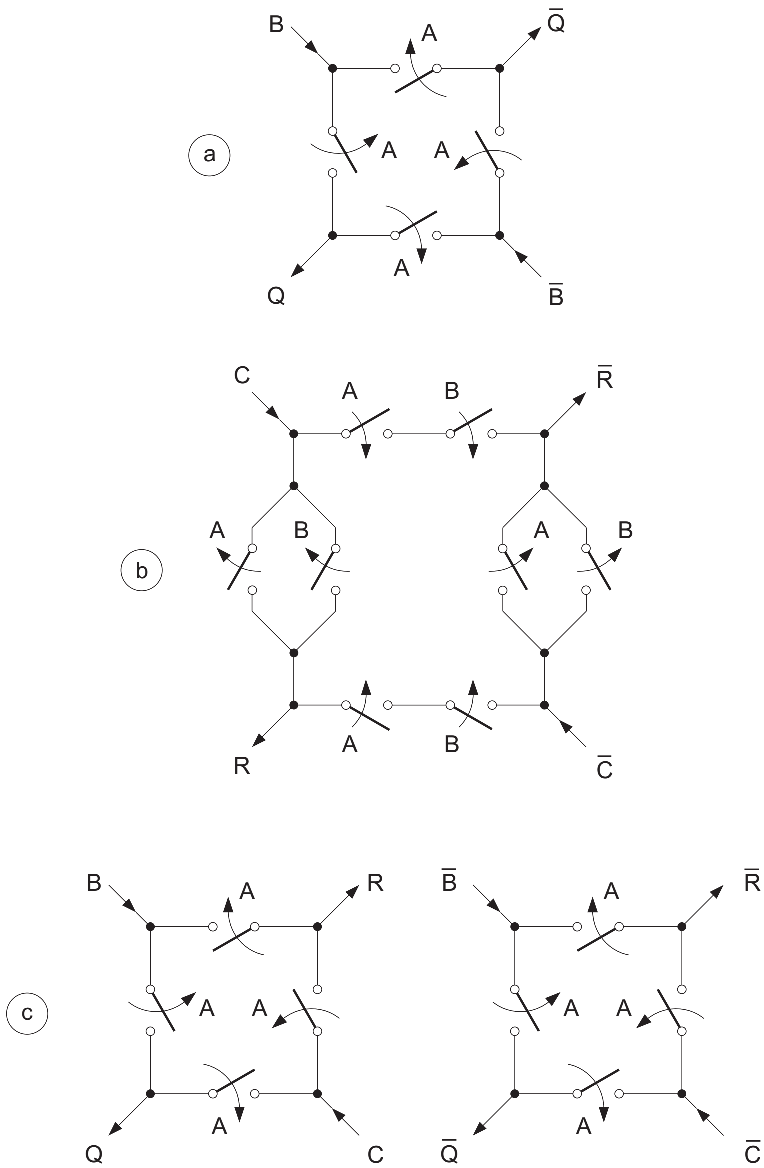
$$\begin{aligned} P &= A \\ Q &= B \\ R &= \textbf{if } (AB = 0) \textbf{ then } C \textbf{ else } \overline{C} \ . \end{aligned}$$

Schematic for

(a) `CONTROLLED NOT` **gate**

(b) `CONTROLLED CONTROLLED NOT` **gate**

(c) `CONTROLLED SWAP` **gate**

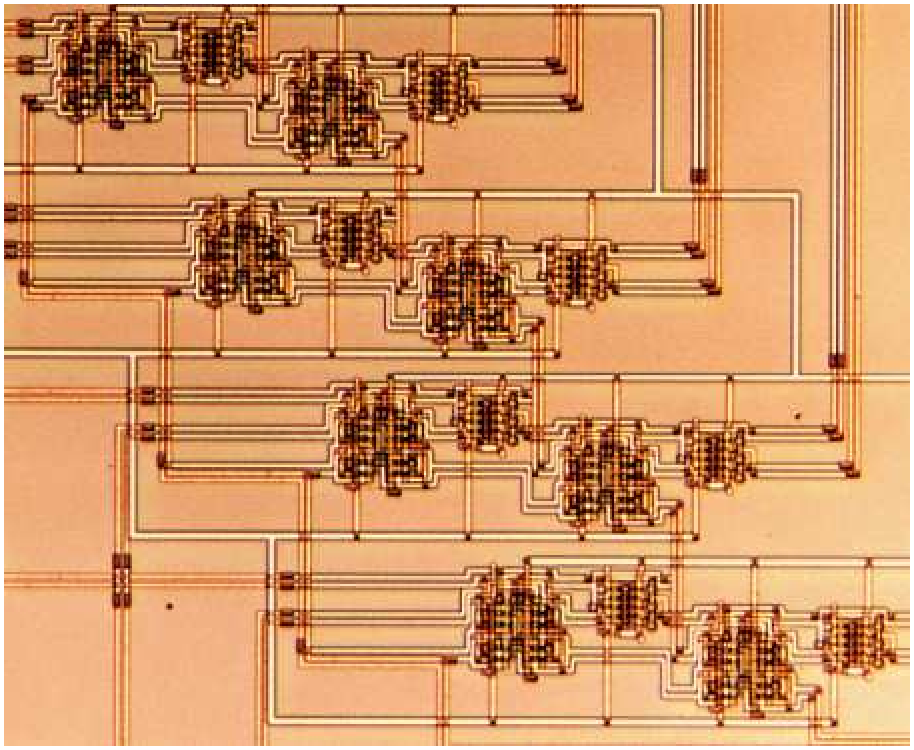


Transistor cost:

The `CONTROLLED NOT` **gate :**
8 transistors

The `CONTROLLED CONTROLLED NOT` **gate or** `TOFFOLI` **gate :**
16 transistors

The `CONTROLLED SWAP` **gate or** `FREDKIN` **gate :**
16 transistors.



Microscope photograph (140 μm $\times$ 120 μm) of 2.4-μm 4-bit reversible ripple adder (192 transistors).

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Truth table of full adder
(a) irreversible
(b) reversible

ABC_{in}	$C_{out}S$
0 0 0	0 0
0 0 1	0 1
0 1 0	0 1
0 1 1	1 0
1 0 0	0 1
1 0 1	1 0
1 1 0	1 0
1 1 1	1 1

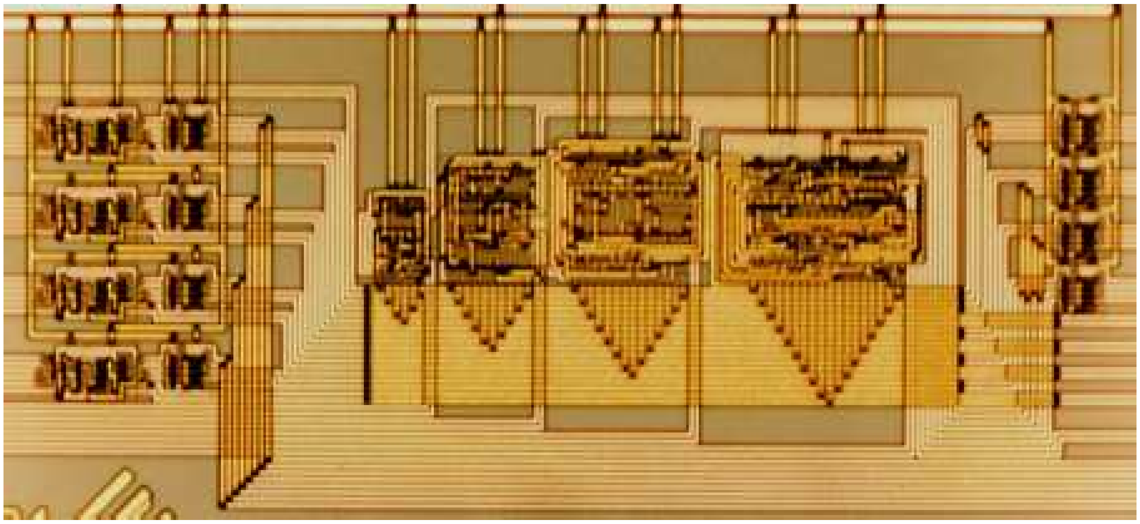
(a)

A	B	C_{in}	P	C_{out}	S	G_1	G_2
0	**0**	**0**	0	**0**	**0**	0	0
0	0	0	1	1	0	0	0
0	**0**	**1**	0	**0**	**1**	0	0
0	0	1	1	1	1	0	0
0	**1**	**0**	0	**0**	**1**	0	1
0	1	0	1	1	1	0	1
0	**1**	**1**	0	**1**	**0**	0	1
0	1	1	1	0	0	0	1
1	**0**	**0**	0	**0**	**1**	1	1
1	0	0	1	1	1	1	1
1	**0**	**1**	0	**1**	**0**	1	1
1	0	1	1	0	0	1	1
1	**1**	**0**	0	**1**	**0**	1	0
1	1	0	1	0	0	1	0
1	**1**	**1**	0	**1**	**1**	1	0
1	1	1	1	0	1	1	0

(b)

Thus : one extra input bit : preset P

and two extra output bits : garbages G_1 **and** G_2



Microscope photograph (610 μm $\times$ 290 μm) of 0.8-μm 4-bit reversible carry-look-ahead adder (320 transistors).

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Truth table of Boolean function $f(A, B, C)$
(a) irreversible
(b) reversible

ABC	f
0 0 0	0
0 0 1	0
0 1 0	0
0 1 1	1
1 0 0	0
1 0 1	1
1 1 0	1
1 1 1	1

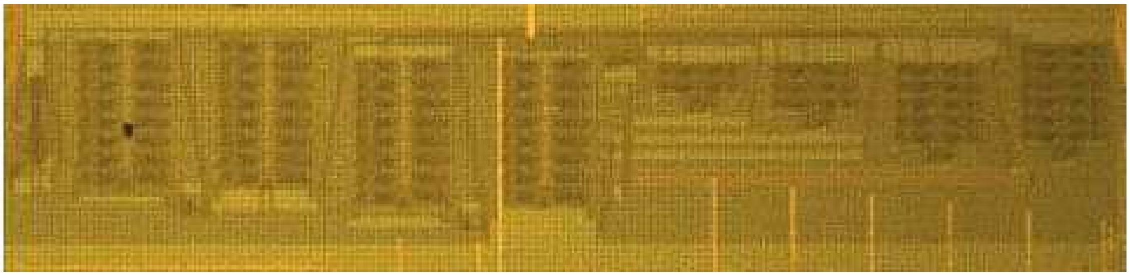
(a)

A	B	C	P	G_1	G_2	G_3	$f \oplus P$
0	**0**	**0**	0	0	0	0	**0**
0	0	0	1	0	0	0	1
0	**0**	**1**	0	0	0	1	**0**
0	0	1	1	0	0	1	1
0	**1**	**0**	0	0	1	0	**0**
0	1	0	1	0	1	0	1
0	**1**	**1**	0	0	1	1	**1**
0	1	1	1	0	1	1	0
1	**0**	**0**	0	1	0	0	**0**
1	0	0	1	1	0	0	1
1	**0**	**1**	0	1	0	1	**1**
1	0	1	1	1	0	1	0
1	**1**	**0**	0	1	1	0	**1**
1	1	0	1	1	1	0	0
1	**1**	**1**	0	1	1	1	**1**
1	1	1	1	1	1	1	0

(b)

Thus : one extra input bit : preset P

and MANY extra output bits : garbages G_i



Microscope photograph (1,430 μm $\times$ 300 μm) of 0.35-μm 8-bit reversible multiplier (2,504 transistors).

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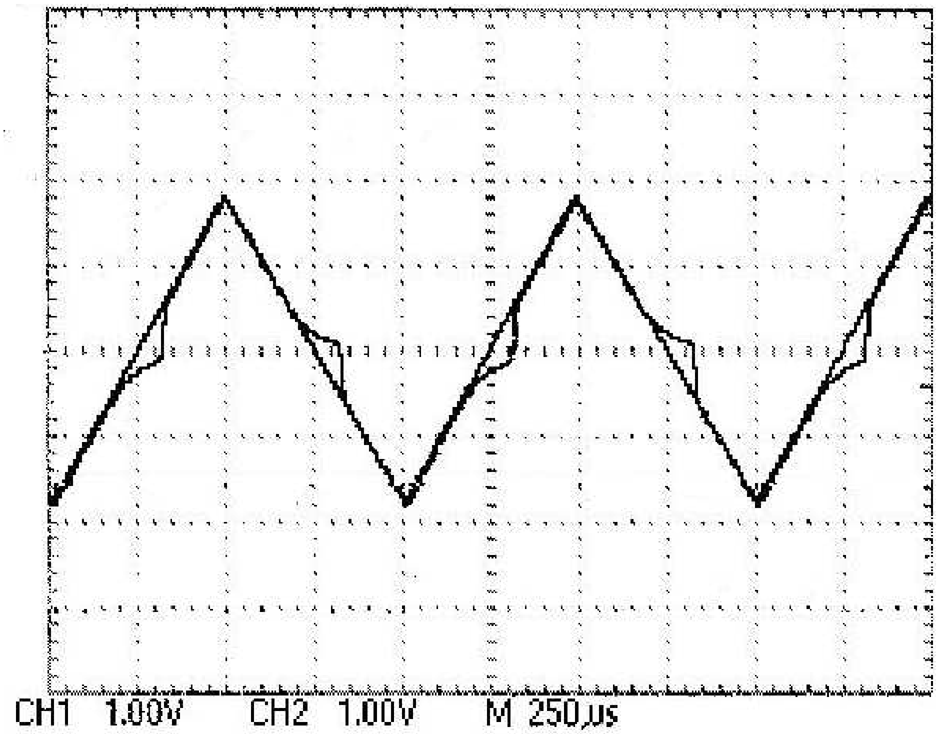
Microscope photograph (140 μm $\times$ 230 μm) of 0.35-μm 8-bit Cuccaro adder (2002) (392 transistors).



Oscilloscope view of 0.35 μm full adder.

Moore's law for
dimensions L, W, and t
threshold voltage V_t
heat dissipation Q

technology (μm)	L (μm)	W (μm)	t (nm)	V_t (V)	Q (f J)
2.4	2.4	2.4	42.5	0.9	38
0.8	0.8	2.0	15.5	0.75	2.0
0.35	0.35	0.5	7.4	0.6	0.30

Energy dissipation per computational step:

$$Q \approx C V_t^2 \ ,$$

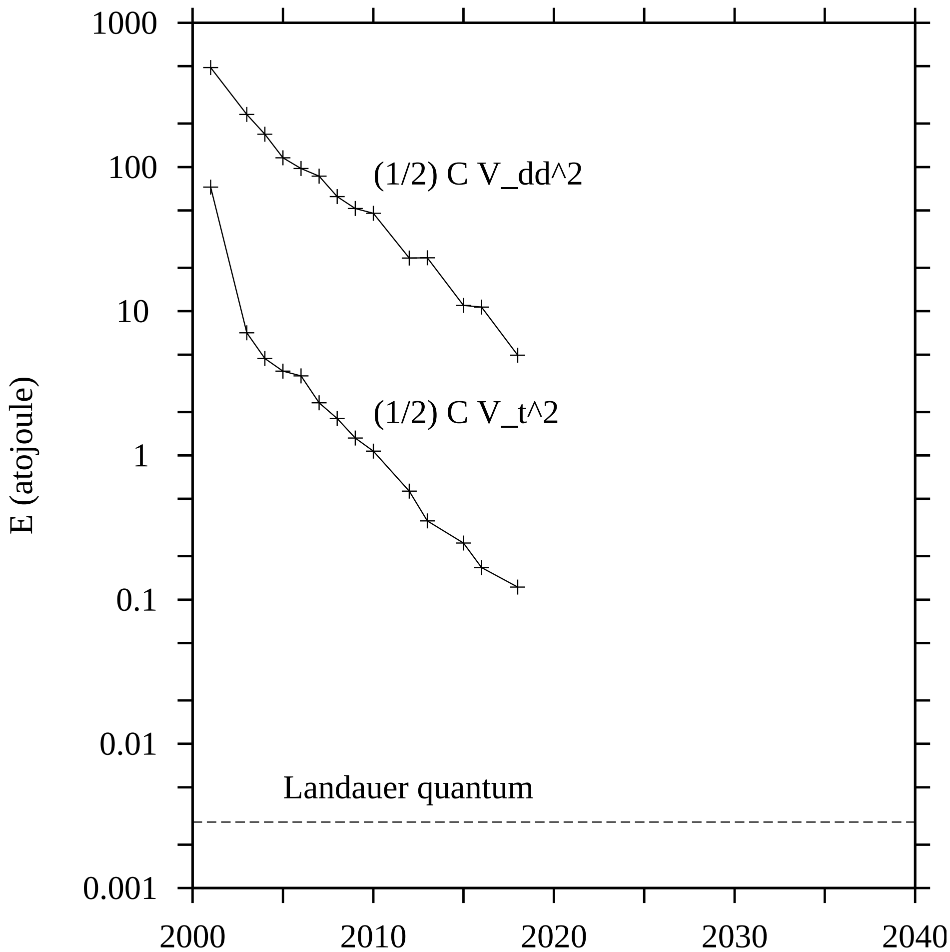
where

$$C \approx \epsilon_0 \, \epsilon \, \frac{W L}{t}$$

We compare with the Landauer quantum

$$kT \log(2) \approx 3 \ \mathbf{z\,J} = \mathbf{0.000\ 003\ f\,J} \ .$$

C = **transistor capacitance**
V_{dd} = **power-supply voltage**
V_t = **transistor threshold voltage**



A perspective from the 2003 ITRS
= International Technology Roadmap of Semiconductors.